Efficient Universal Quantum Circuits

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Abstract. We define and construct efficient depth-universal and almost-size-universal quantum circuits. Such circuits can be viewed as general-purpose simulators for central quantum circuit classes and used to capture the computational power of the simulated class. For depth we construct universal circuits whose depth is the same order as the circuits being simulated. For size, there is a log factor blow-up in the universal circuits constructed here which is nearly optimal for polynomial size circuits.

1 Introduction

Quantum computing is most naturally formulated using the quantum circuit model [Y93]. Many quantum algorithms are expressed in terms of (uniform) special-purpose circuits which depend strongly on the problem being solved. However, the notion of a universal quantum computer is more naturally captured by quantum Turing machines [D85]. This being the case, it is desirable to have a notion of efficient universal quantum circuits in the spirit of universal quantum Turing machines.

Like resource-bounded universal Turing machines, efficiently constructed universal circuits characterize the hardest languages computed by circuits in a given circuit class. The existence of a universal circuit family for a complexity class defined by resource bounds (depth, size, gate width, etc.) provides an upper bound on the resources needed to compute any circuit in that class. More precisely, the specific, efficient construction of a universal circuit for a class of circuits with a fixed input length, yields a single circuit which can be used to carry out the computation of every circuit in that class, basically a chip or processor for that class of circuits. The more efficient the universal circuit, the smaller and faster the processor for that class. For example, depth-universal circuits are desirable

because they can simulate any circuit within a constant slow-down factor. Thus they are as time-efficient as possible.

Universal quantum circuits have been studied before in different contexts. Most of the research on universal quantum circuit classes deals with finding universal sets of gates which can be used to efficiently simulate any quantum computation ([NC00], [SR07]). Our goal is quite different; we want to create a circuit which, like a computer, takes as input both a program and data and runs the program on the data. Nielsen and Chuang [NC97] considered a similar problem, although they did not focus on efficiency of the universal circuit. They showed that it is not possible for a generic universal circuit to work for all circuits of a certain input length. We avoid this problem by considering families of circuits with a certain depth or size, constructed from a fixed family of gates.

In the case of quantum circuits there are particular issues relating to the requirements that computations must be clean and reversible which come into play, and to an extent complicate the classical methods. Still, much of our motivation for this work originates with classical results due to Cook, Valiant, and others [CH85,V76]. Cook and Hoover considered depth universality and described a depth-universal uniform circuit family for circuits of depth $\Omega(\log n)$. Valiant studied size universality and showed how to construct universal circuits of size $O(s \log s)$ to simulate any circuit of size s. (See Sect. 1.1).

Definition 1 (Universal Quantum Circuits). *Fix $n > 0$ and let $\mathcal{C}$ be a collection of quantum circuits on n qubits. A quantum circuit U on $n + m$ qubits is* universal *for $\mathcal{C}$ if, for every circuit $C \in \mathcal{C}$, there is a string $x \in \{0,1\}^m$ (the encoding) such that for all strings $y \in \{0,1\}^n$ (the data),*

$$U(|y\rangle \otimes |x\rangle) = C|y\rangle \otimes |x\rangle.$$

The circuit collections we are interested in are usually defined by bounding various parameters such as the size (number of gates), depth (number of layers of gates acting simultaneously on disjoint sets of qubits), or palette of allowed gates (e.g., Hadamard, $\pi/8$, CNOT).

As in the classical case, we also want our universal circuits to be *efficient* in various ways. For one, we restrict them to using the same gate family as the circuits they simulate. We may also want to restrict their size or the number m of qubits they use for the encoding. We are particularly concerned with the depth of universal circuits. Depth-universal circuits are desirable because they can simulate any circuit within a constant slow-down factor. Thus they are as time-efficient as possible.

Definition 2 (Depth-Universal Quantum Circuits). *Fix a family $\mathcal{F}$ of unitary quantum gates. A family of quantum circuits $\{U_{n,d}\}_{n,d>0}$ is* depth-universal *over $\mathcal{F}$ if*

1. *$U_{n,d}$ is universal for n-qubit circuits with depth $\leq d$ using gates from $\mathcal{F}$,*
2. *$U_{n,d}$ only uses gates drawn from $\mathcal{F}$,*
3. *$U_{n,d}$ has depth $O(d)$, and*

4. the number of encoding qubits of $U_{n,d}$ is polynomial in n and d.

Our first result, presented in Sect. 3, shows that depth-universal quantum circuits exist for the gate families $\mathcal{F} = \{H, T\} \cup \{F_n \mid n \geq 1\}$ and $\mathcal{F}' = \{H, T\} \cup \{F_n \mid n \geq 1\} \cup \{\wedge_n(X) \mid n \geq 1\}$, where H and T are the Hadamard and $\pi/8$ gates, respectively, and F_n and $\wedge_n(X)$ are the $(n+1)$-qubit fanout and $(n+1)$-qubit Toffoli gates, respectively (see Sect. 2).

In order to construct efficient universal circuit families, it appears necessary to resort to the massive parallelism that fanout gates[4] provide; note that the existing classical constructions make abundant use of fanout which is a very natural operation for classical circuits. It is an open question whether the same efficiency can be achieved without using fanout gates.

Theorem 1. *Depth-universal quantum circuits exist over $\mathcal{F}$ and over $\mathcal{F}'$. Such circuits use $O(n^2 d)$ qubits and can be built log-space uniformly in n and d.*

Note that the results for the two circuit families are independent, because it is not known whether n-qubit Toffoli gates can be implemented exactly in constant depth using single-qubit gates and fanout gates, although they can be approximated this way [HS05]. It would be nice to find depth-universal circuits over families of bounded-width gates[5] such as $\{H, T, \text{CNOT}\}$. A simple connectivity argument shows that depth-universal circuits with bounded-width gates, if they exist, must have depth $\Omega(\log n)$ and thus can only depth-efficiently simulate circuits with depth $\Omega(\log n)$. One can therefore only hope to find depth-universal circuits for circuits of depth $\Omega(\log n)$ over bounded-width gates. Although such circuits exist in the classical case (see below), we are unable to construct them in the quantum case (see Sect. 5).

1.1 Other relevant work

The study of quantum circuit complexity was originated by Yao [Y93]. The basic definitions and first results in this research area can be found in Nielsen and Chuang [NC00].

Cook and Hoover [CH85] considered the problem of constructing general-purpose classical (Boolean) circuits using gates with fanin two. They asked whether, given n, c, d, there is a circuit U of size $c^{O(1)}$ and depth $O(d)$ that can simulate any n-input circuit of size c and depth d. Cook and Hoover constructed a depth-universal circuit for depth $\Omega(\log n)$ and polynomial size, but which takes as input a nonstandard encoding of the circuit, and they also presented a circuit with depth $O(\log n \log \log n)$ to convert the standard encoding of the circuit to the required encoding. Valiant looked at a similar problem— trying to minimize the size of the universal circuit [V76]. He considered classical circuits built from fanin 2 gates (but with unbounded fanout) and embedded the circuit in a larger universal graph. He managed to create universal graphs for different types of circuits and showed how to construct a $O(c \log c)$-size and

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[4] The fanout gate is a quantum analog of the classical fanout operation. See Sect. 2.
[5] The width of a gate is the number of qubits it acts upon.

$O(c)$-depth universal circuit. He also showed that his constructions have size within a constant multiplicative factor of the information theoretic lower bound.

For quantum circuits, Nielsen and Chuang (in [NC97]) considered the problem of building what they call *programmable universal gate arrays*. These generic universal circuits work on two quantum registers, a data register and a program register. In addition to results mentioned previously, they showed that it is possible to construct an extremely weak type of probabilistic universal circuit with size linear in the number of inputs to the simulated circuit.

Sousa and Ramos considered a similar problem of creating a universal quantum circuit to simulate any quantum gate [SR07]. They construct a basic building block which can be used to implement any single-qubit or CNOT gate on n qubits by switching certain gates on and off. They showed how to combine several of these building blocks to implement any n-qubit quantum gate.

2   Preliminaries

For the rest of the paper, we will use U to denote the universal circuit and C to denote the circuit being simulated. We assume the standard notions of quantum states, quantum circuits, and quantum gates described in [NC00], in particular, H (Hadamard), T ($\pi/8$), $S = T^2$ (phase), and CNOT (controlled NOT). We will also need some additional gates, which we now motivate.

The depth-universal circuits we construct require the ability to feed the output of a single gate to many other gates. While this operation, commonly known as fanout, is common in classical circuits, copying an arbitrary quantum state unitarily is not possible in quantum circuits due to the no-cloning theorem [NC00]. It turns out that we can construct our circuits using a classical notion of fanout operation, defined as the *fanout gate*

$$F_n : |c, t_1, \ldots, t_n\rangle \mapsto |c, c \oplus t_1, \ldots, c \oplus t_n\rangle$$

for any of the standard basis states $|c\rangle$ (the control) and $|t_1\rangle, \ldots, |t_n\rangle$ (the targets) and extended linearly to other states[6] [FFGHZ06]. F_n can be constructed in depth $\lg n$ using CNOT gates. We need to use unbounded fanout gates to achieve full depth universality. We also use the *unbounded Toffoli gate* $\wedge_n(X) : |c_1, \ldots, c_n, t\rangle \mapsto |c_1, \ldots, c_n, t \oplus \bigwedge_{i=1}^{n} c_i\rangle$. We reserve the term "Toffoli gate" to refer to the (standard) Toffoli gate $\wedge_2(X)$, which is defined on three qubits.

In addition to the fanout gate, our construction requires us to use controlled versions of the gates used in the simulated circuit. For most of the commonly used basis sets of gates (e.g., Toffoli gate, Hadamard gate, and phase gate S), the gates themselves are sufficient to construct their controlled versions (e.g., a controlled Hadamard gate can be constructed using a Toffoli gate and Hadamard and phase gates). Depth or size universality requires that the controlled versions of the gates should be constructible using the gates themselves within proper depth or size, as required.

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[6] This does not contradict the no-cloning theorem as only classical states are copied.

Definition 3 (Closed under controlled operation). *A set of quantum gates* $G = \{G_1, \ldots\}$ *is said to be* closed under controlled operation *if for each $G_i \in G$, the controlled version of the gate $C\text{-}G_i|c\rangle|t\rangle \longrightarrow |c\rangle G_i^c|t\rangle$ can be implemented in constant depth and size using the gates in G. Here, $|c\rangle$ is a single qubit and G_i could be a single or a multi-qubit gate.*

Note that CNOT $= F_1$, and given H, T, and CNOT we can implement the Toffoli gate via a standard constant-size circuit [NC00]. We can implement the phase gate S as T^2, and since $T^8 = I$, we can implement $S^\dagger = T^6$ and $T^\dagger = T^7$.

A *generalized Z gate*, which we will hereafter refer to simply as a *Z gate*, is an extension of the single-qubit Pauli Z gate ($|x\rangle \mapsto (-1)^x|x\rangle$) to multiple qubits:

$$|x_1, \cdots, x_n\rangle \overset{Z}{\mapsto} (-1)^{x_1 x_2 \cdots x_n}|x_1, \ldots, x_n\rangle.$$

A Z gate can be constructed easily (in constant depth and size) from a single unbounded Toffoli gate (and vice versa) by conjugating the target qubit of the unbounded Toffoli gate with H gates (i.e., placing H on both sides of the Toffoli gate on its target qubit).

Similarly, a *Z-fanout gate Z_n* applies the single-qubit Z gate to each of n target qubits if the control qubit is set:

$$|c, t_1, \cdots, t_n\rangle \overset{Z_n}{\mapsto} (-1)^{c \cdot (t_1 + \cdots + t_n)}|c, t_1, \ldots, t_n\rangle.$$

A Z_n gate can be constructed from a single F_n gate and vice versa in constant depth (although not constant size) by conjugating each target with H gates. So, in our depth-universal circuit construction, we can use either or both of these types of gates. Similarly for unbounded Toffoli versus Z gates. Z gates and Z-fanout gates are convenient to work with because they only change the phase, leaving the values of the qubits intact (they are represented by diagonal matrices in the computational basis). This allows us to use a trick due to Høyer and Špalek [HS05] and run all possible gates for a layer in parallel.

3 Depth-universal quantum circuits

In this section, we prove Theorem 1, i.e., that depth-universal circuits exist for each of the gate families

$$\mathcal{F} = \{H, T\} \cup \{F_n \mid n \geq 1\},$$
$$\mathcal{F}' = \{H, T\} \cup \{F_n \mid n \geq 1\} \cup \{\wedge_n(X) \mid n \geq 1\}.$$

We first give the proof for $\mathcal{F}$ then show how to modify it for $\mathcal{F}'$.

The depth-universal circuit U we construct simulates the input circuit C layer by layer, where a layer consists of the collection of all its gates at a fixed depth. C is encoded in a slightly altered form, however. First, all the fanout gates in C are replaced with Z-fanout gates on the same qubits with H gates conjugating the targets. At worst, this may roughly double the depth of C (adjacent H gates cancel). Each layer of the resulting circuit is then separated into three adjacent

layers: the first having only the H gates of the original layer, the second only the T gates, and the third only the Z-fanout gates. U then simulates each layer of the modified C by a constant number of its own layers. We describe next how these layers are constructed.

Simulating single-qubit gates. The circuit to simulate an n-qubit layer of single-qubit gates of type G, say, consists of a layer of controlled-G gates where the control qubits are fed from the encoding and the target qubits are the data qubits. Figure 1 shows a layer of G gates, where $G \in \{H, T\}$, controlled using H, S, T, CNOT, and Toffoli gates. To simulate G gates on qubits $i_1, \ldots, i_k$, say, set $c_{i_1}, \ldots, c_{i_k}$ to 1 and the rest of the c-qubits to 0.
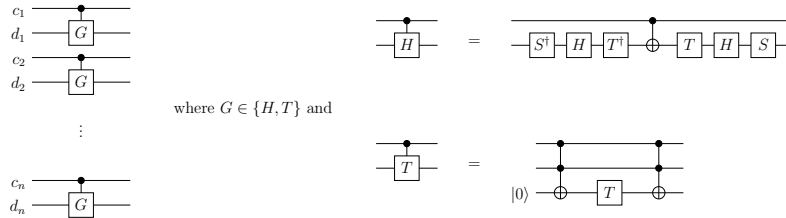

Fig. 1. Simulating a layer of single-qubit G gates with controlled G gates. The ancilla in the implementation of the controlled T gate is assumed part of the encoding. The ancilla is reset to 0 at the end and hence can be reused for implementing all T layers.

Simulating Z-fanout gates. The circuit to simulate a Z-fanout layer is shown in Figure 2.
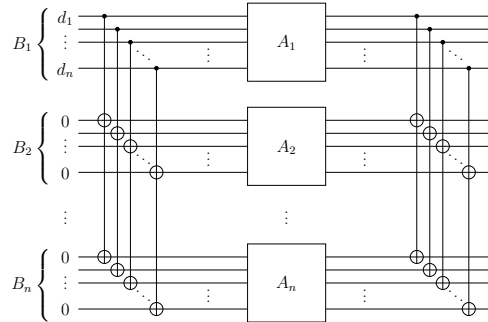

Fig. 2. Simulating a layer of Z-fanout gates.

The top n qubits are the original data qubits. The rest are ancilla qubits. All the qubits are arranged in n blocks $B_1, \ldots, B_n$ of n qubits per block. The qubits in block B_i are labeled $b_{i1}, \ldots, b_{in}$. Each A_i subcircuit looks like Figure 3. The qubits $c_{i1}, \ldots, c_{in}$ are encoding qubits. The large gate between the two columns of Toffoli gates is a Z-fanout gate with its control on the ith ancilla (corresponding to b_{ii} and c_{ii}) and targets on all the other ancillæ.

Here is the state evolution from $|\boldsymbol{d}\rangle = |d_1 \cdots d_n\rangle$, suppressing the c_{ij} qubits and ancillæ internal to the A_i subcircuits in the ket labels. Note that after the
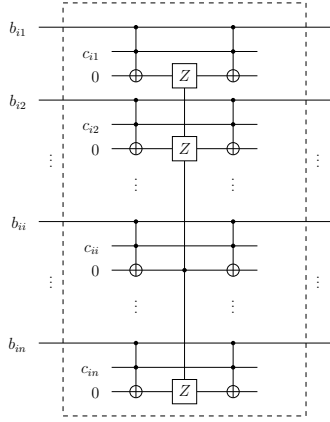
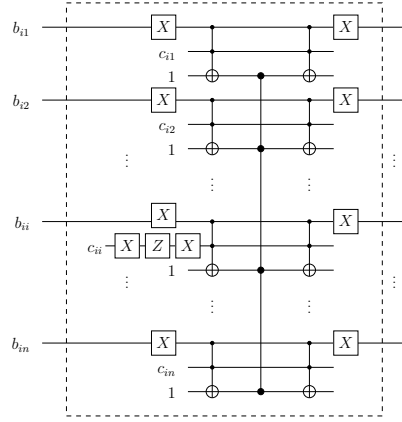**Fig. 3.** Subcircuit A_i in the simulation of Z-fanout gates.

Fig. 4. Subcircuit A_i for a layer of Z gates.

first layer of fanouts, each qubit b_{ij} carries the value d_j.

$$|\boldsymbol{d}, \boldsymbol{0}, \ldots, \boldsymbol{0}\rangle \mapsto |\boldsymbol{d}, \boldsymbol{d}, \ldots, \boldsymbol{d}\rangle$$
$$\mapsto (-1)^{\sum_i d_i c_{ii}\left(\sum_{j \neq i} d_j c_{ij}\right)}|\boldsymbol{d}, \boldsymbol{d}, \ldots, \boldsymbol{d}\rangle$$
$$\mapsto (-1)^{\sum_i d_i c_{ii}\left(\sum_{j \neq i} d_j c_{ij}\right)}|\boldsymbol{d}, \boldsymbol{0}, \ldots, \boldsymbol{0}\rangle.$$

To simulate some Z-fanout gate G of C whose control is on the ith qubit, say, we do this in block B_i by setting c_{ii} to 1 and c_{ij} to 1 for every j where the jth qubit is a target of G. All the other c-qubits in B_i are set to 0. We can do this in separate blocks for multiple Z-fanout gates on the same layer, because no two gates can share the same control qubit. Any c-qubits in unused blocks are set to 0.

Simulating unbounded Toffoli gates. We modify the construction above to accommodate unbounded Toffoli gates (family $\mathcal{F}'$), or equivalently Z gates, by breaking each layer of C into four adjacent layers, the first three being as before, and the fourth containing only Z gates. The top-level circuit to simulate a layer of Z gates is as before (Figure 2) and each A_i subcircuit looks like Figure 4, where the central gate is a Z gate connecting the ancillæ. To simulate a Z gate G of C whose first qubit is i, say, we do this in block B_i by setting c_{ii} to 1 and setting c_{ij} to 1 for every j where the jth qubit is part of G. All the other c-qubits in B_i are set to 0. As before, we do this in separate blocks for multiple gates on the same layer, since no two gates can share the same first qubit. Any c-qubits in unused blocks are set to 0, and it is easy to check that this makes the block have no net effect.

4 Size-universal quantum circuits

Similar to a depth-universal circuit, a *size-universal circuit* is a universal circuit with the same order of the number of gates as the circuit it is simulating. Formally,

Definition 4. *A family $\{U_{n,c}\}$ of universal circuits for n-qubit circuits of size $\leq c$ is* size-universal *if $SIZE(U_{n,c}) = O(c)$.*

Via a simple counting argument, it is not possible to obtain a completely size-universal circuit for fanin-2 circuits. The number of possible circuits with c fanin-2 gates is $\Omega((n-1)^{c+1})$. Since all the encoding bits have to be connected to some of the fanin-2 gates in the universal circuit, it must have $\Omega(c \log n)$ gates.

We use Valiant's idea of universal graphs [V76] to construct a universal family of fanin-2 circuits that are very close to the aforementioned lower bound. As before, we would like to simulate C by using the same set of gates used in C. Our construction works for any circuit using unbounded Toffoli gates and any set of single-qubit and 2-qubit gates closed under the controlled operation.

The graph of any circuit of size n can be represented as a directed acyclic graph with vertices $\{1, \ldots, n\}$ such that there is no edge from j to i for $i < j$ and each vertex has fanin and fanout 2. Let $\Gamma_2(n)$ be the set of all such graphs.

Definition 5 (Edge-universal graph [V76]). *A graph G' is* edge-universal *for $\Gamma_2(n)$ if it has distinct vertices (poles) $p_1, \ldots, p_n$ such that any graph $G \in \Gamma_2(n)$ can be embedded into G' where each vertex $i \in G$ is mapped to distinct vertex $\rho(i) = p_i \in G'$ and distinct edges $(i,j) \in E$ are mapped to edge-disjoint paths $rho(i) \rightsquigarrow \rho(j) \in E'$.*

Theorem 2 (Universal graph[V76]). *There is a constant k such that for all n there exists an acyclic graph G' that is edge-universal for $\Gamma_2(n)$, and G' has $kn \lg n$ vertices, each vertex having fanin and fanout 2.*

It is fairly easy to construct a universal circuit using the universal graph. Consider any edge-universal graph G' for $\Gamma_2(n + c)$. Then G' has $c' = k(n + c) \log(n + c)$ vertices for some k. These c' vertices include poles $p_1, \ldots, p_{n+c}$ and non-pole vertices. Create a corresponding quantum circuit C' with c' gates (including the inputs). For each of the vertices $p_1, \ldots, p_n$ of G', remove their incoming edges and replace the vertices by the input as shown in Figure 5. Replace each of the vertices $p_{n+1}, \ldots, p_{n+c}$ with a subcircuit that applies any of the single- or 2-qubit gates on the inputs, where the gate to apply is controlled by the encoding (Figure 7 shows an example). For a non-pole vertex, replace it with a subcircuit that swaps the incoming and outgoing wires (i.e., first input is connected to second output and second input is connected to first output) or directly connects them (i.e., first input is connected to first output and similarly for the second input) depending on the encoding (see Figure 6). The edge disjointness property guarantees that wires in the embedded circuit are mapped to paths in C' which can share a vertex but cannot share any edge.

To simulate any fanin-2 circuit C with c gates acting on n qubits, construct the edge-universal graph G' for $\Gamma_2(n + c)$. Embed the graph of C into G' such that the input nodes of C are mapped to the poles $p_1, \ldots, p_n$ in G'. Now for each gate of the circuit, set a bit in the encoding to denote the type of the gate at that pole to which it was mapped. For the non-pole vertices, set a bit in the encoding to specify whether the two input values should be swapped or mapped directly to the two output values.
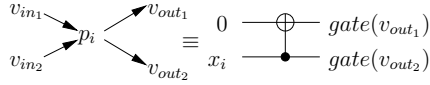
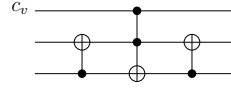**Fig. 5.** The gate for a pole vertex p_i is mapped to input x_i.

Fig. 6. The gates at a non-pole vertex v. The encoding bit c_v specifies if first output qubit should be mapped to first input or second input qubit and similarly for second output qubit.
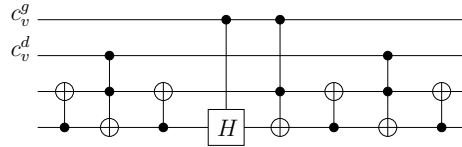

Fig. 7. Example of the gates at a pole vertex v simulating a circuit with CNOT and H gates. The encoding bits c_v^g specify which kind of gate is at vertex v, and the c_v^d specify which qubit the gate acts on (for H gate) or which is the control qubit (for CNOT gate).

Theorem 3. *There is a constant k and a family of universal circuits $U_{n,c}$ that can simulate every circuit with c gates acting on n qubits such that $SIZE(U_{n,c}) = O((n+c)\log(n+c))$.*

For unbounded fanin circuits, if we can decompose the unbounded fanin gates into linearly many bounded fanin gates, then a similar idea can be used.

Corollary 1. *There is a family of universal circuits $U_{n,c}$ that can simulate quantum circuits of size c on n qubits and consisting of Hadamard, $\pi/8$, and unbounded Toffoli gates such that $SIZE(U_{n,c}) = O(nc\log(nc))$.*

5 Conclusions

We have been mostly concerned with the actual simulation of a quantum circuit C by the universal circuit U. However, it is possible to hide some complexity of the simulation in U's description of C itself. Usually, the description of a classical circuit is the underlying graph of the circuit and specifies the gates at each vertex. But we use a grid description of quantum circuits which is more natural and especially suitable for simulation; in the description the rows of the grid correspond to the qubits, and the columns correspond to the different layers of the circuit. A graph-based description can be easily converted to this grid-based description in polynomial time.

The techniques of Sect. 3 can be easily adapted to build depth-universal circuits for a variety of classical (Boolean) circuit classes with unbounded gates, e.g., AC, ACC, and TC circuits. The key reason is that these big gates are all

"self-similar" in the sense that fixing some of the inputs can yield a smaller gate of the same type.

A number of natural, interesting open problems remain.

Fanout gates are used in our construction of a depth-universal circuit family. Is the fanout gate necessary in our construction? We believe it is. In fact, we do not know how to simulate depth-d circuits over $\{H, T, \mathrm{CNOT}\}$ universally in depth $O(d)$ without using fanout gates, even assuming that the circuits being simulated have depth $\Omega(\log n)$. The shallowest universal circuits with bounded-width gates we know of have a $\lg n$ blow-up factor in the depth, just by replacing the fanout gates with log-depth circuits of CNOT gates.

Our results apply to circuits with very specific gate sets. How much can these gate sets be generalized? Are similar results possible for any countable set of gates containing Hadamard, unbounded Toffoli, and fanout gates?

We showed how to contruct a universal circuit with a logarithmic blow-up in size. The construction is within a constant factor of the minimum possible size for polynomial-size, bounded-fanin circuits. However for constant-size circuits, we believe the lower bound can be tightened to match the proven upper bound.

Acknowledgments

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